Please add new claims 19-23 as follows:

--19 (new) A method for manufacturing a semiconductor device according to claim 15, wherein the etching a portion of the second conducting layer also forms a first resistance element and a second resistance element in the analog element region.

20. (new) A method as in claim 19, further comprising performing at least one ion-implantation of an impurity into part of the second conducting layer prior to the etching a portion of the second conducting layer.

21. (new) A method as in claim 20, wherein a number of ion-implantations of impurity in a region where the first resistance element is to be formed is greater than a number of ion-implantations of impurity in a region where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

22. (new) A method as in claim 19, wherein, prior to the etching a portion of the second conducting layer, an impurity is diffused in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

23. (new) A method as in claim 19, wherein prior to the etching a portion of the second conducting layer, a silicide layer is formed in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.--